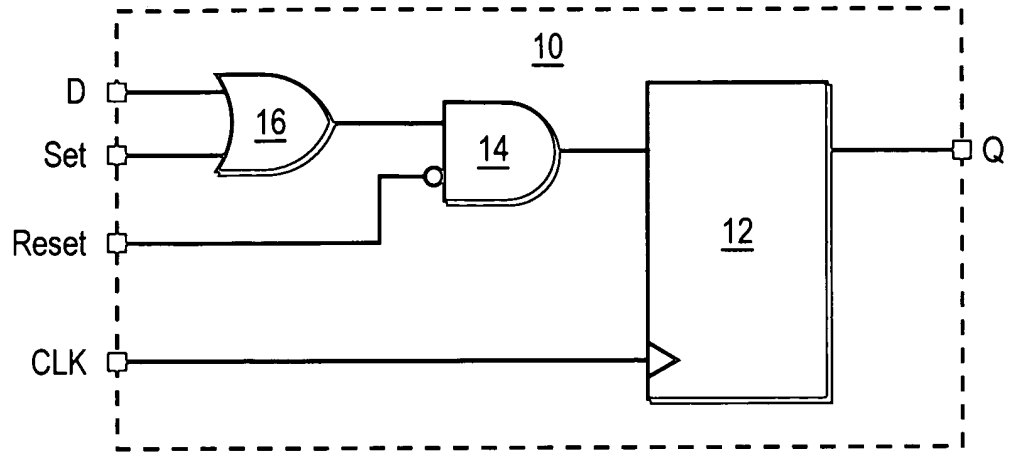

FIG. 1

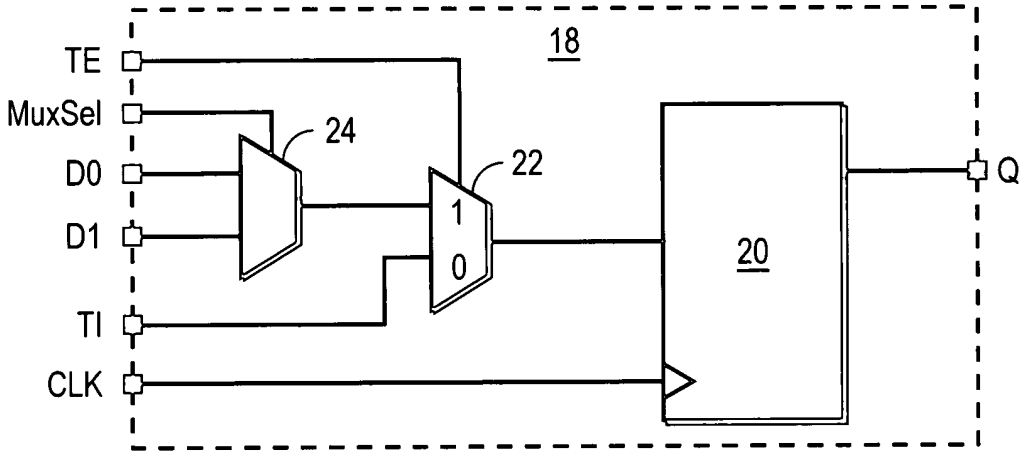

FIG. 2

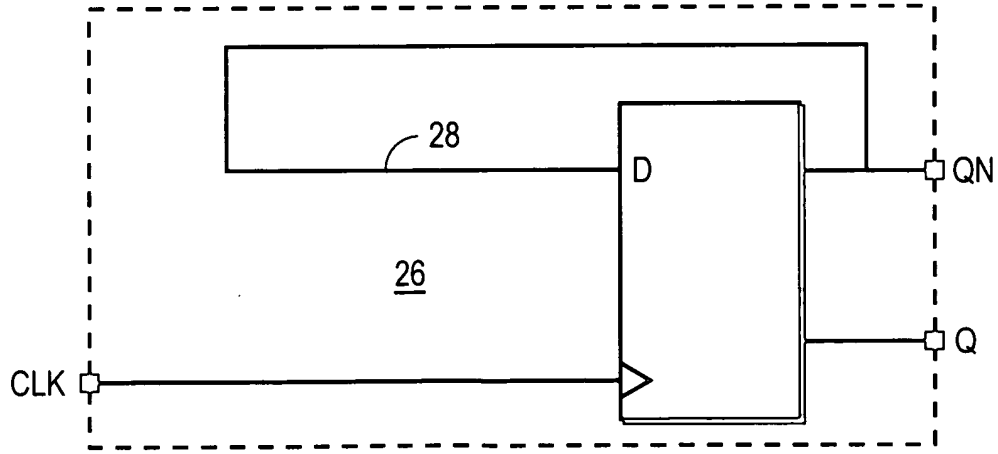

FIG. 3

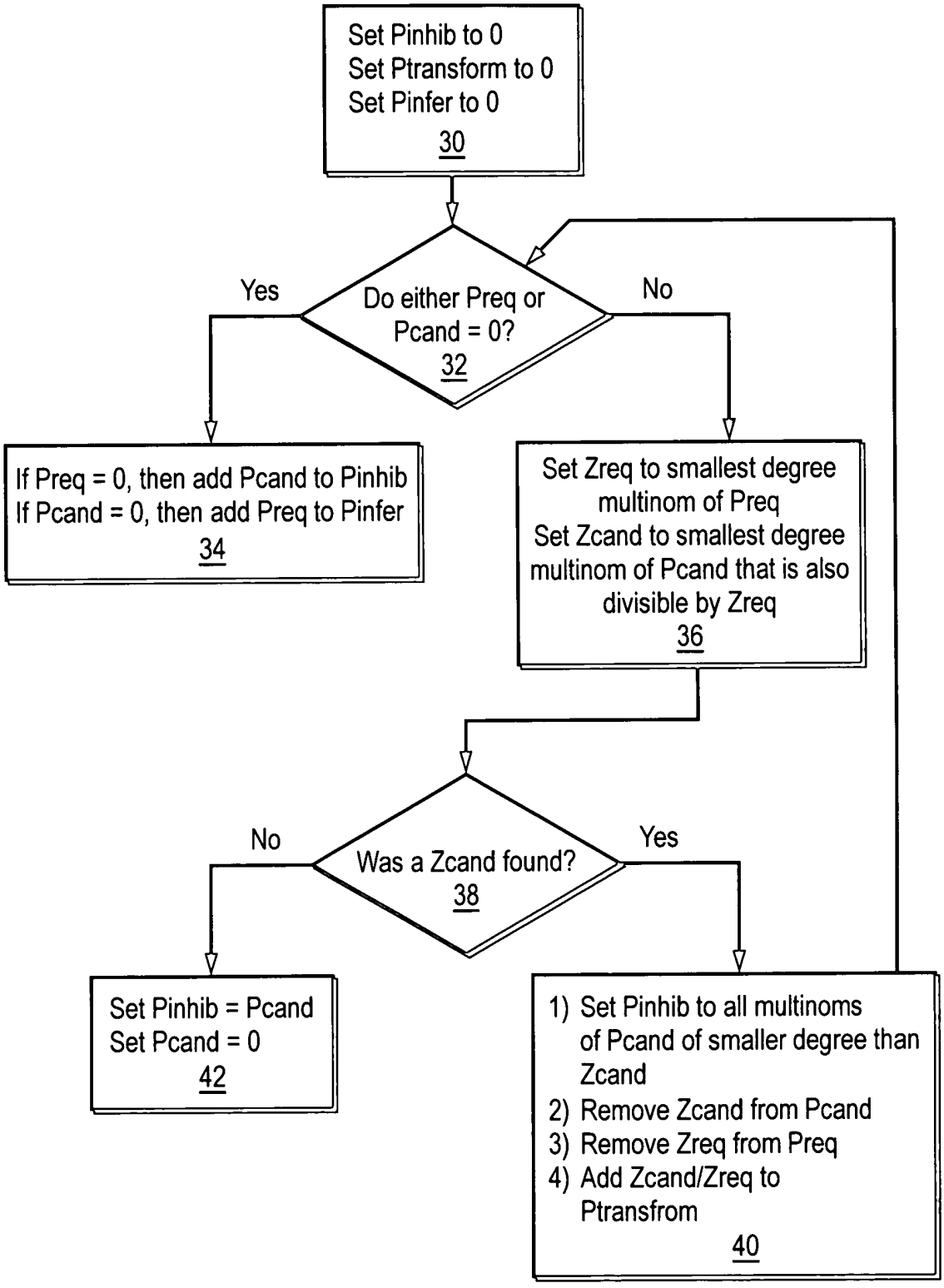
Set Pinhib to 0
Set Ptransform to 0
Set Pinfer to 0
30
Do either Preq or Pcand = 0?
32
Yes
No
If Preq = 0, then add Pcand to Pinhib
If Pcand = 0, then add Preq to Pinfer
34
Set Zreq to smallest degree multinom of Preq
Set Zcand to smallest degree multinom of Pcand that is also divisible by Zreq
36
Was a Zcand found?
38
No
Yes
Set Pinhib = Pcand
Set Pcand = 0
42
1) Set Pinhib to all multinoms of Pcand of smaller degree than Zcand
2) Remove Zcand from Pcand
3) Remove Zreq from Preq
4) Add Zcand/Zreq to Ptransfrom
40

FIG. 4

Inhibition	
Rst	inhib a Reset active high
RstLr	inhib a Reset active low
St	inhib a Set active high
StLs	inhib a Set active low
ScStRst	inhib a Scan active high
ScStLsRstLc	inhib a Scan active low
MuScStRst	inhib a Mux
Re	inhib a Recirculating active high
ReLre	inhib a Recirculating active low
T	stop proces, impossible to inhib a Toggle element

FIG. 5

Transformation	
rule 1	**1**: Do nothing
rule 2	**Ls or Ls^-1**: Add an inverter on the Reset terminal
rule 3	**Lr or Lr^-1**: Add an inverter on the Set terminal
rule 4	**Lre or Lre^-1**: Add an inverter on the Recirculating enable
rule 5	**LrLs or (LrLs)^-1**: Add an inverter on the Scan enable
rule 6	**ScSt**: set TI to Vss and connect TE to Reset terminal
rule 7	**ScRst**: set TI to Vss and connect TE to Set terminal
rule 8	**ScRst(Ls^-1)**: set TI to Vdd and connect TE to set terminal with an inverter
rule 9	**ScSt(Lr^-1)**: set TI to Vss and connect TE to reset terminal with an inverter
rule 10	**ScStLrLs**: set TI to Vss and connect TE to reset terminal with an inverter
rule 11	**ScRstLrLs**: set TI to Vdd and connect TE to set terminal with an inverter
rule 12	**ScRstLr**: set TI to Vdd and connect TE to set terminal
rule 13	**ScStLs**: set TI to Vss and connect TE to reset terminal
rule 14	**Mu**: connect D1 to TI and connect SEL to TE terminal
rule 15	**Mu(LrLs)^-01**: connect D0 to TI and connect SEL to TE terminal
rule 16	**MuScSt**: set D1 to Vss and connect SEL to Reset terminal
rule 17	**MuScRst**: set D1 to Vdd and connect SEL to set terminal
rule 18	**MuScRst(Ls^-1)**: set D0 to Vdd and connect SEL to set terminal
rule 19	**MuScSt(Lr^-1)**: set D0 to Vss and connect SEL to set terminal
rule 20	**Mu^-1)**: connect D1 to TI, SEL to TE
rule 21	**(Mu^-1)LsLr**: connect D0 to TI, SEL to TE

FIG. 6

Inference	
Rst	infer a Reset active high
RstLr	infer a Reset active low
St	infer a Set active high
StLs	infer a Set active low
ScStRst	infer a Scan active high
ScStLsRstLr	infer a Scan active low
MuScStRst	infer a Mux
Re	infer a Recirculating active high
ReLre	infer a Recirculating active low
T	infer a Toggle element

FIG. 7

row/column	Rst	RstLR	St	StLs	ScStRst	ScStLsRstLr	MuScStRst	Re	ReLre	T
Rst	T1	T2	-----	-----	-----	-----	-----	-----	-----	-----
RstLr	T2	T1	-----	-----	-----	-----	-----	-----	-----	-----
St	-----	-----	T1	T3	-----	-----	-----	-----	-----	-----
StLs	-----	-----	T3	T1	-----	-----	-----	-----	-----	-----
ScStRst	T6	T9	T7	T8	T1	T5	T20	-----	-----	-----
ScStLsRstLr	T10	T13	T11	T12	T5	T1	T21	-----	-----	-----
MuScStRst	T16	T19	T17	T18	T14	T15	T1	-----	-----	-----
Re	-----	-----	-----	-----	-----	-----	-----	T1	T4	-----
ReLre	-----	-----	-----	-----	-----	-----	-----	T4	T1	-----
T	-----	-----	-----	-----	-----	-----	-----	-----	-----	T1

FIG. 8

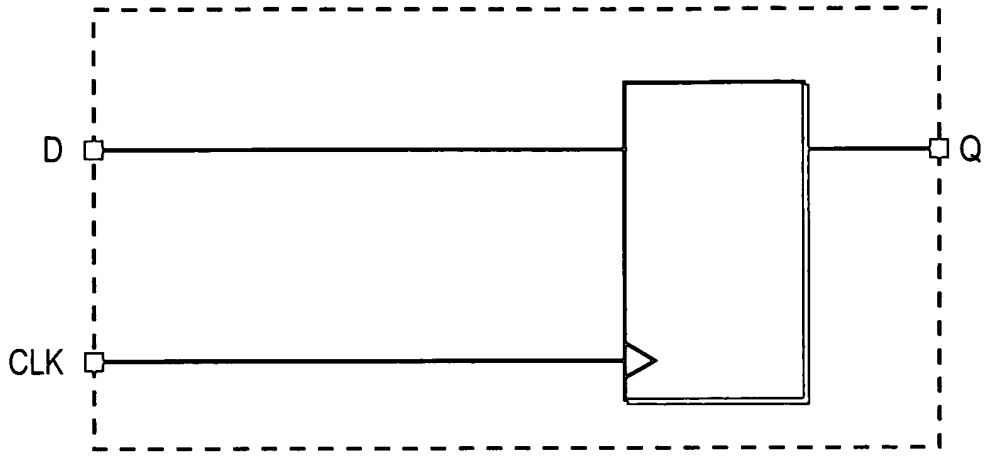

FIG. 9

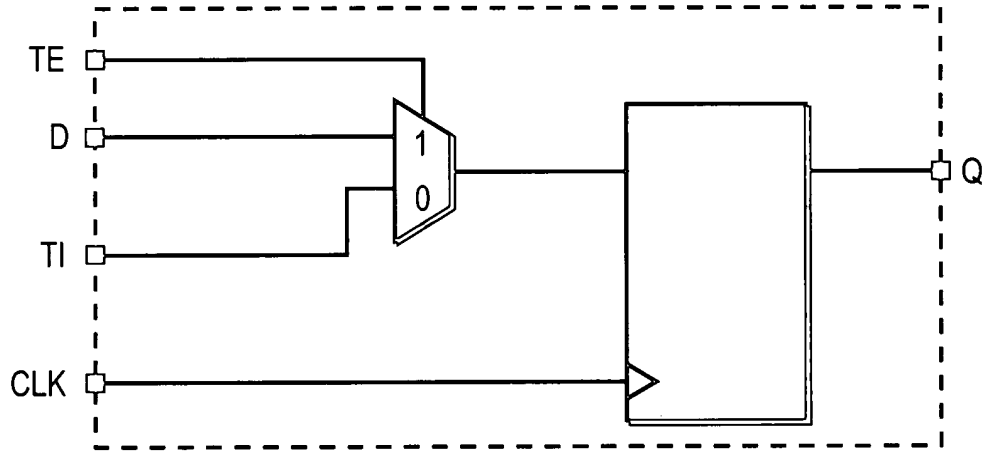

FIG. 10

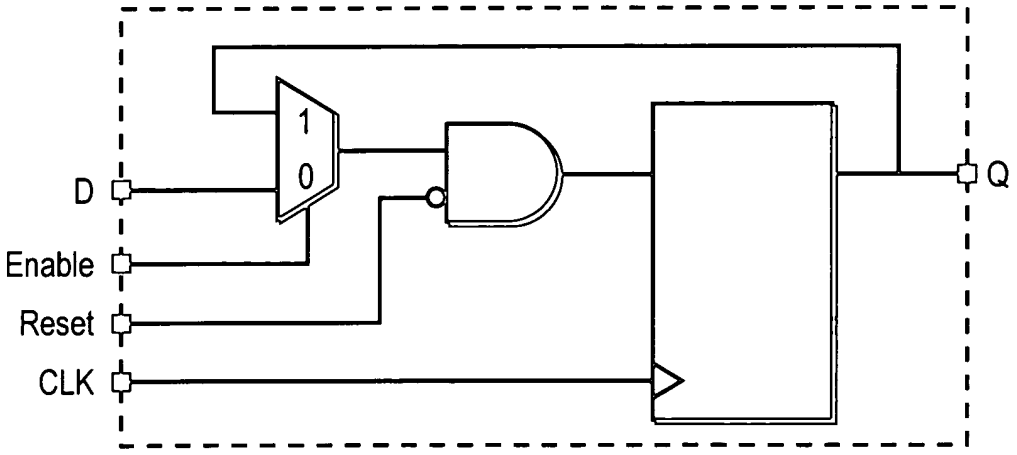

FIG. 11